layer (e.g., the metal layer **254**), and forming a second glass layer (e.g., the glass layer **252**).

[0047] The method **500** may include forming a second electrode, at **510**. For example, one or more of the electrodes **160**, **260** may be formed by depositing a conductive material (e.g., tungsten) on the wafer.

[0048] Although not depicted in FIG. **5**, the method **500** may include one or more additional processes, such as one or more deposition process or one or more etching process. Further, additional layers and structures (e.g., insulating layers, metal routing layers, via structures, and spacer structures) may be formed on or between the layers described herein.

[0049] Referring to FIG. **6**, a flow chart depicting an embodiment of a method **600** of forming a variable resistance memory device where an active layer includes germanium-telluride is depicted. The method **600** may include forming a first electrode, at **602**. For example, the electrodes **310** may be formed by depositing a conductive material on a semiconductor wafer.

[0050] The method **600** may further include forming an active layer by co-sputtering carbon with germanium-telluride, at **604**. For example, the active layer **330** may be formed by co-sputtering carbon with germanium-telluride. Alternatively, one or more other doping process may be used to introduce the carbon into the germanium-telluride.

[0051] The method **600** may also include forming an ion source structure, at **606**. For example, the ion source structure **350** may be formed by forming a depositing a first glass layer (e.g., the glass layer **351**), forming a metal layer (e.g., the metal layer **354**), and forming a second glass layer (e.g., the glass layer **356**).

[0052] The method **600** may include forming a second electrode, at **608**. For example, the electrodes **360** may be formed by depositing a conductive material (e.g., tungsten) on the wafer.

[0053] Although various embodiments have been shown and described, the present disclosure is not so limited and will be understood to include all such modifications and variations as would be apparent to one skilled in the art having the benefit of this disclosure. Further, it should be understood that the disclosure is not intended to be limited to the particular forms disclosed. Rather, the intention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the disclosure as defined by the appended claims.

1. A variable resistance memory device comprising:
- a first electrode and a second electrode;
- a chalcogenide glass layer between the first electrode and the second electrode, the chalcogenide glass layer including a chalcogenide glass material co-deposited with a metal material;
- a metal ion source structure between the chalcogenide glass layer and the second electrode; and
- a buffer layer between the first electrode and the chalcogenide glass layer, wherein the buffer layer includes the chalcogenide glass material and excludes the metal material.

2. The device of claim **1**, wherein the metal material includes chromium, tungsten, copper, cobalt, indium, or a combination thereof.

3. The device of claim **1**, wherein the chalcogenide glass material includes germanium selenide.

4. (canceled)

5. The device of claim **1**, wherein the metal ion source structure includes:
- a first adhesion layer and a second adhesion layer; and
- a mobile metal layer between the first adhesion layer and the second adhesion layer.

6. The device of claim **5**, wherein the first adhesion layer and the second adhesion layer include the chalcogenide glass material.

7. The device of claim **5**, wherein the metal layer includes silver.

8. The device of claim **5**, wherein a thickness of the metal layer is between 600 Å and 1000 Å.

9. The device of claim **5**, wherein a thickness of the first adhesion layer and the second adhesion layer is less than 200 Å.

10. The device of claim **1**, further comprising a metal-chalcogenide layer between the chalcogenide glass layer and the metal ion source structure.

11. The device of claim **10**, wherein the metal chalcogenide layer includes tin-selenide.

12. The device of claim **10**, wherein a thickness of the metal chalcogenide layer is between 750 Å and 1250 Å.

13. The device of claim **1**, wherein a thickness of the chalcogenide glass layer is between 250 Å and 35 Å.

14. The device of claim **1**, wherein a thickness of the buffer layer is between 50 Å and 150 Å.

15. The device of claim **1**, further comprising another buffer layer between the chalcogenide glass layer and the metal ion source structure.

16. The device of claim **1**, wherein an electrical resistance between the first electrode and the second electrode is programmable within the range of 10 kΩ and 1 MΩ.

17. The device of claim **1**, wherein an electrical resistance between the first electrode and the second electrode is programmable within the range of 10 kΩ and 100 kΩ.

18. A variable resistance memory device comprising:
- a first electrode and a second electrode;
- a chalcogenide glass layer between the first electrode and the second electrode, the chalcogenide glass layer including germanium-telluride co-deposited with carbon;
- a metal-chalcogenide layer between the chalcogenide glass layer and the second electrode; and
- an ion source structure between the metal-chalcogenide layer and the second electrode.

19. The device of claim **18**, wherein the metal chalcogenide layer comprises a metal-selenide layer, the metal-selenide layer including tin-selenide.

20. The device of claim **18**, wherein the germanium-telluride is co-deposited with carbon using a co-sputtering process.

21. A method of forming a variable resistance memory device, the method comprising:
- forming a first electrode;
- forming a buffer layer;
- forming a chalcogenide glass layer by co-depositing a chalcogenide glass material and a metal material, wherein the buffer layer includes the chalcogenide glass material and excludes the metal material;
- forming an ion source structure; and
- forming a second electrode.